

# Quartus II and DE2 Manual

1) Start the Quartus II software. You should see a display similar to the one in Figure 1.

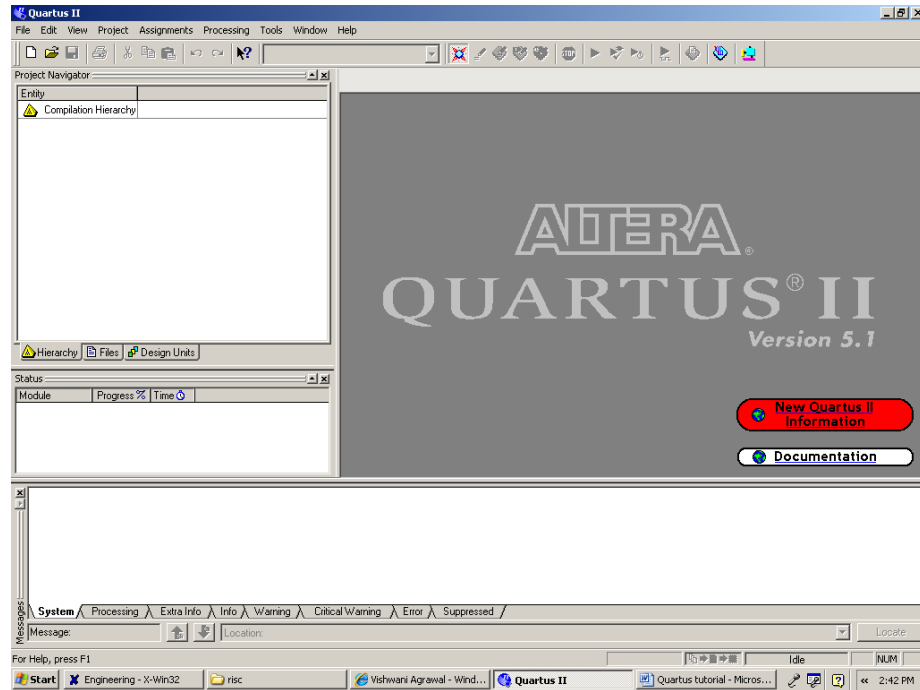


Fig. 1

2) To start working on a new design we first have to define a new design project. Create a new project as follows: Select File >New Project Wizard as shown in Figure 2 to reach the window in Figure 3. You can skip this window. Press Next to get the window shown in Figure 4.

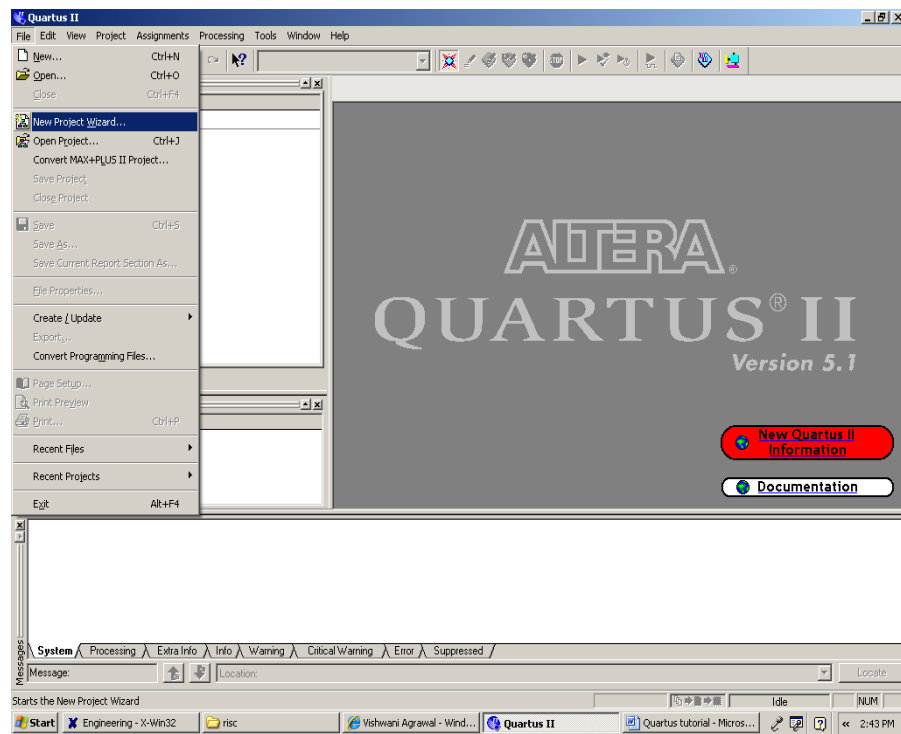


Fig 2

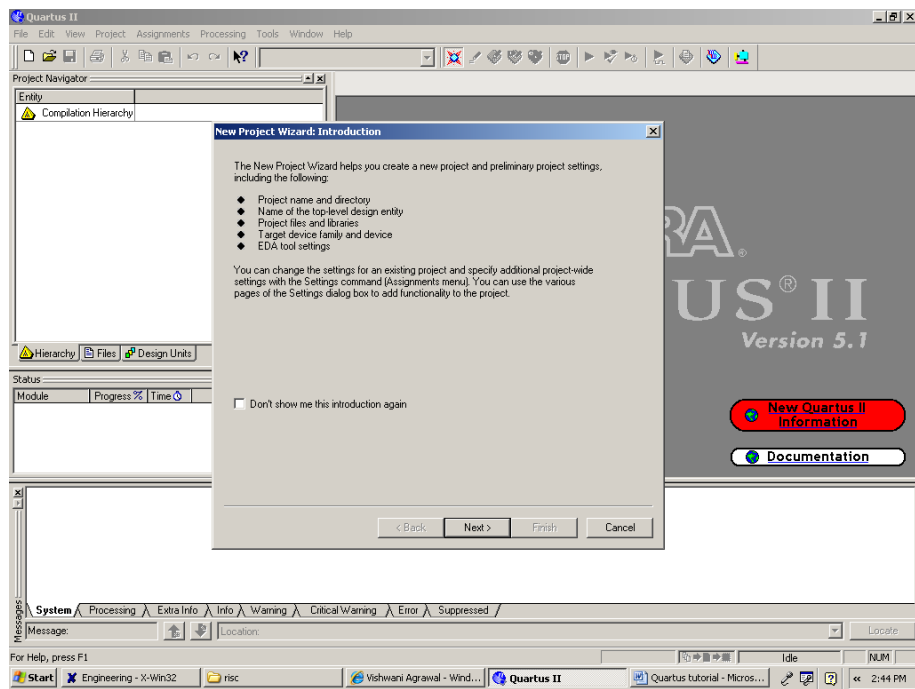


Fig. 3

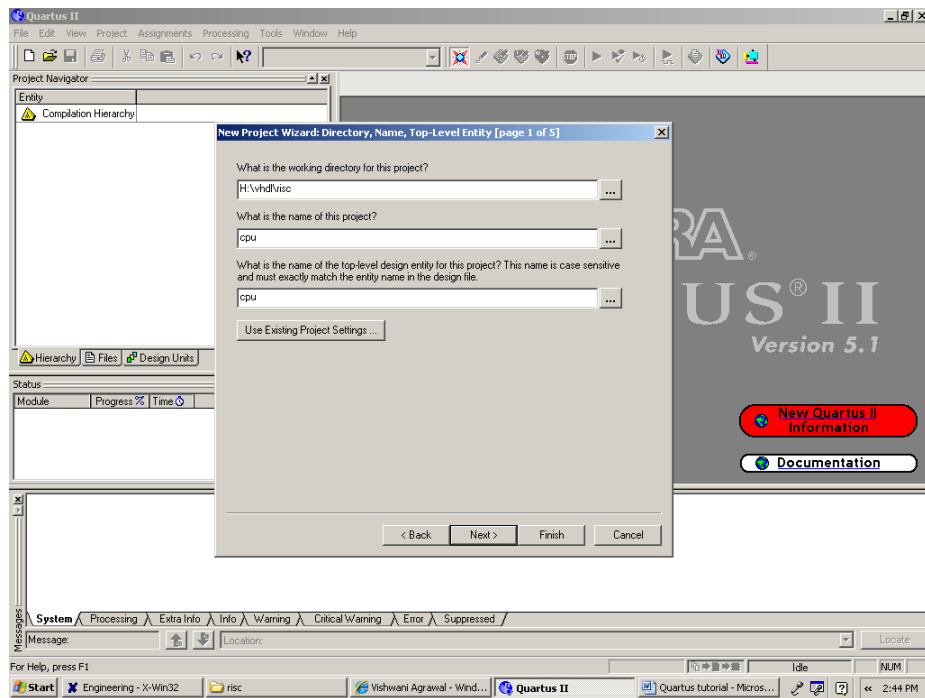


Fig. 4

3) Fill in your working directory name for the project. The project must have a name, which is usually the same as the top-level design entity that will be included in the project. After this click Next to get to the window as shown in Figure 5.

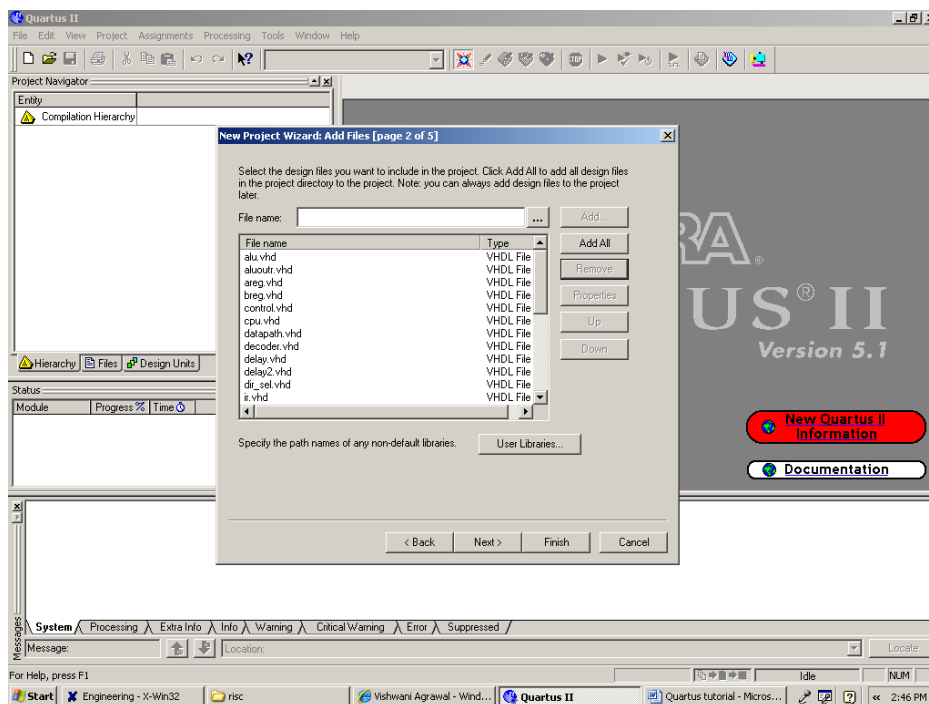


Fig. 5

4) Add all the files that must be included in your project except for the packages and libraries. After that click on the User Libraries icon shown on this window. This will get you to Figure 6.

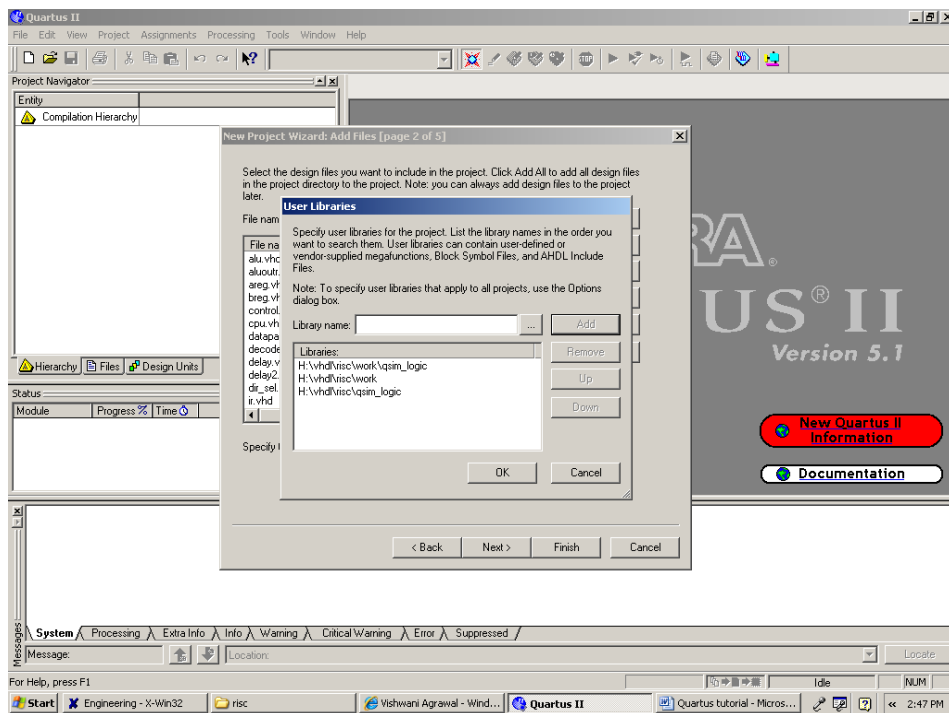


Fig. 6

5) Add all the libraries and packages you have used in your project here. IEEE libraries and packages do not need to be added. Click Ok and upon returning to window in Figure 6 click Next to get to the window as shown in Figure 7.

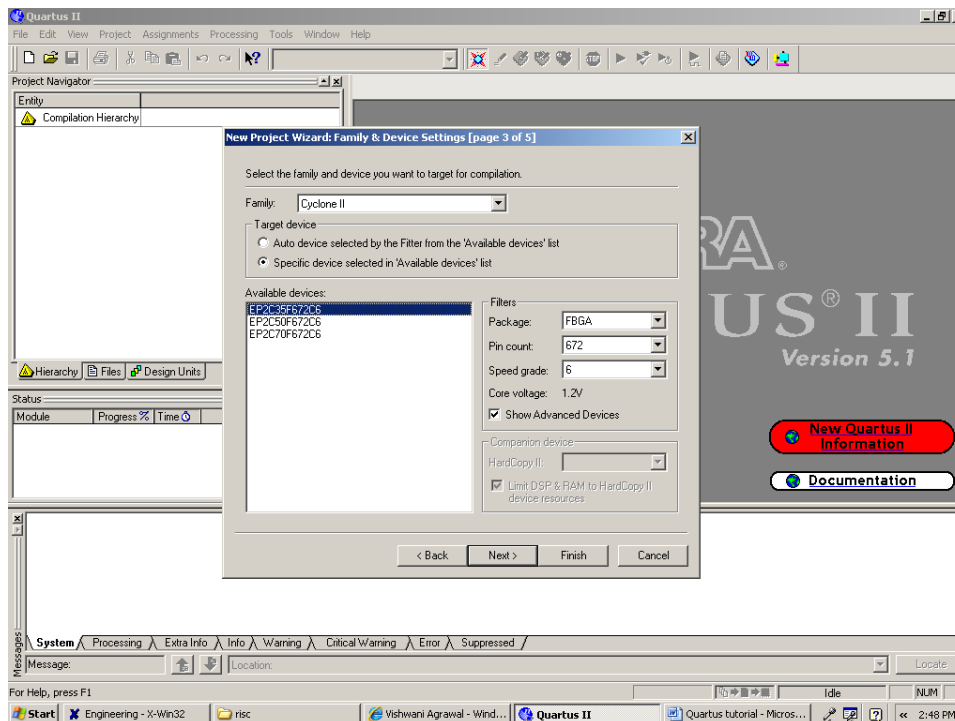


Fig. 7

6) Choose the Device Family name as Cyclone II, pin count 672, speed grade 6, and package FBGA, and from the list of available devices, choose the device called

EP2C35F672C6 which is the FPGA used on Altera's DE2 board. Press Next, which opens the window in Figure 8.

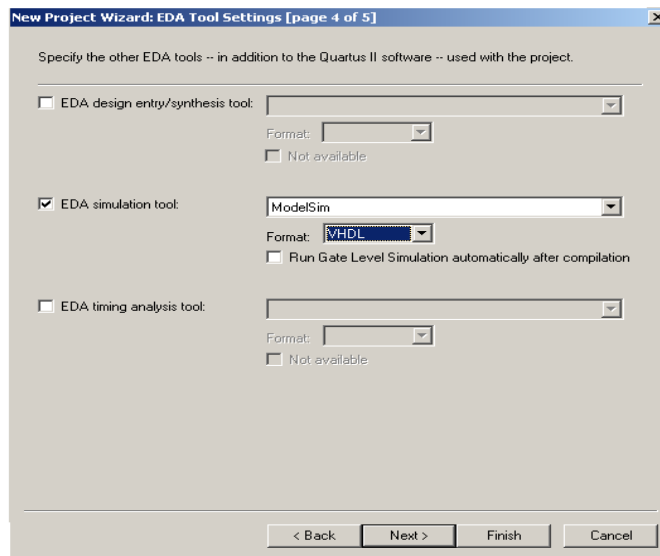


Fig. 8

7) We can specify any third-party tools that should be used for the project. For this project we need to choose the Modelsim(VHDL) tool under the EDA Simulation Tool option. After Selecting this tool press Next.

8) A summary of the chosen settings appears in the screen shown in Figure 9. Press Finish, which returns to the main Quartus II window, but with the new project specified in the display title bar.

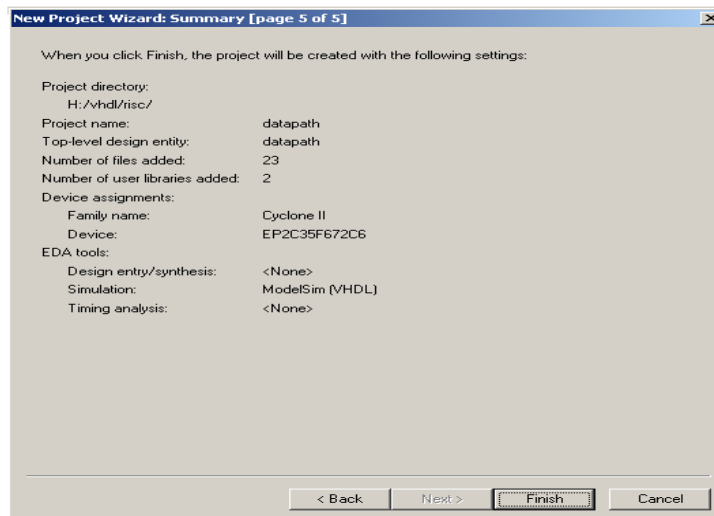


Fig. 9

9) The VHDL code in the file is processed by several Quartus II tools that analyze the code, synthesize the circuit, and generate an implementation of it for the target chip. These tools are controlled by the application program called the *Compiler*. Run the Compiler by selecting Processing >Start Compilation, or by clicking on the toolbar icon that looks like a purple triangle as shown in Figure 10. As the compilation moves through various stages, its progress is reported in a window on the left side of the Quartus II display as shown in Figure 11. Successful (or unsuccessful) compilation is indicated in a pop-up box. Acknowledge it by clicking OK, which leads to the Quartus II display as shown in Figure 12. In the message window, at the bottom of the figure, various messages are displayed. In case of errors, there will be appropriate messages given. When the compilation is finished, a compilation report is produced. This window can be opened at any time either by selecting Processing >Compilation Report or by clicking on the icon. The report includes a number of sections listed on the left side of its window.

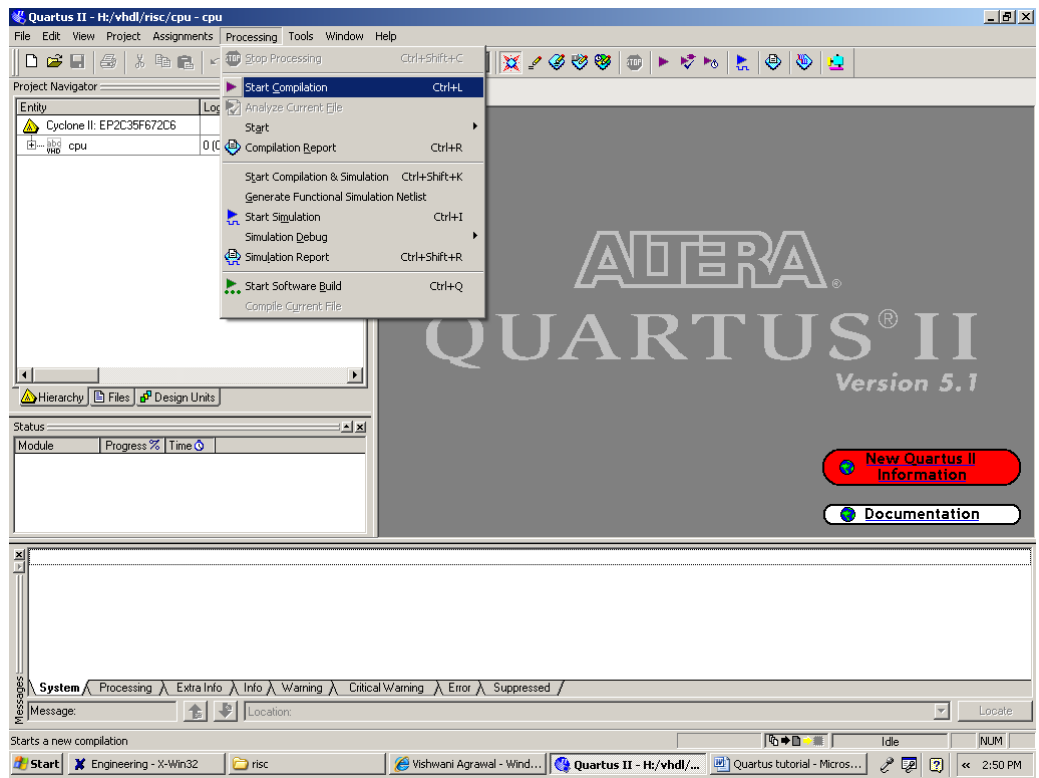


Fig. 10

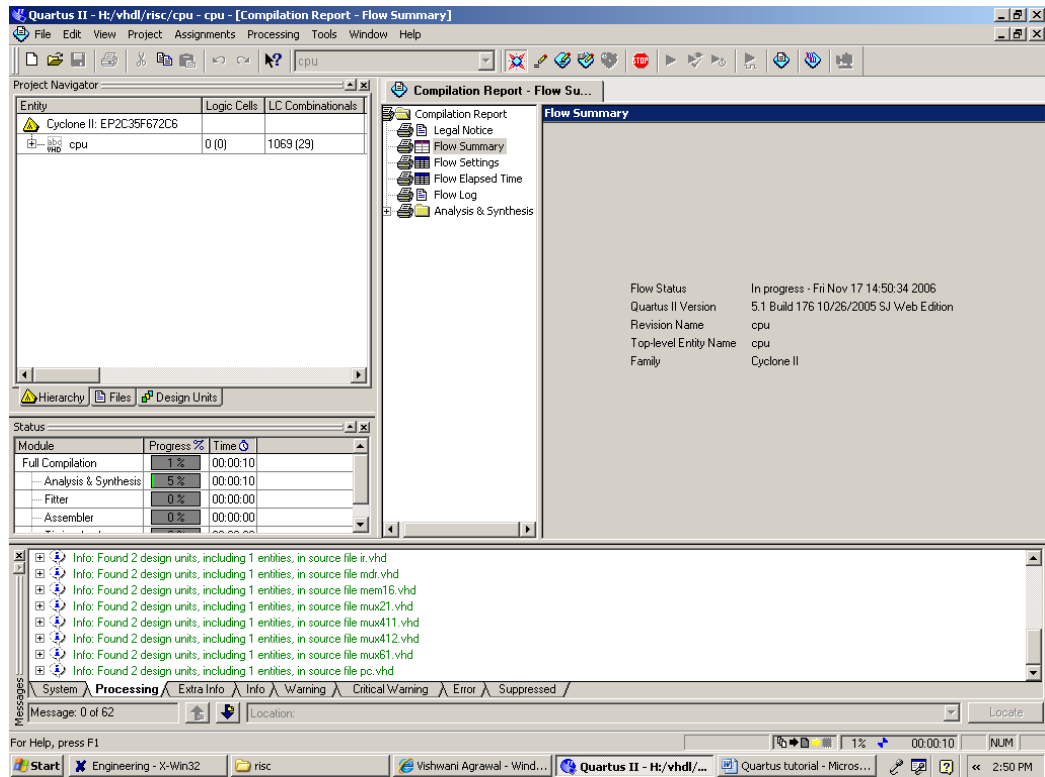


Fig. 11

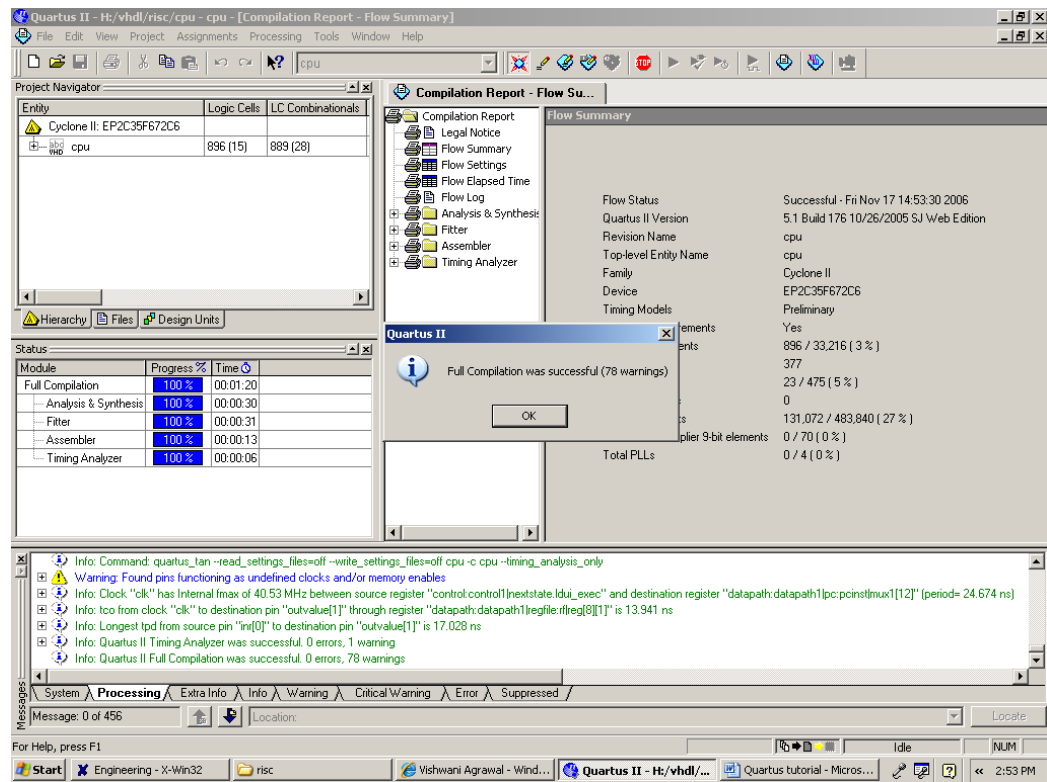


Fig. 12

10) Quartus II software displays messages produced during compilation in the Messages window. If the VHDL design file is correct, one of the messages will state that the compilation was successful and that there are no errors. If the Compiler does not report zero errors, then in that case a message corresponding to each error found will be displayed in the Messages window. Double-clicking on an error message will highlight the offending statement in the VHDL code in the Text Editor window. Similarly, the Compiler may display some warning messages. Their details can be explored in the same way as in the case of error messages. Correct the errors if any and recompile the design.

11) After Compilation is done, Simulation needs to be done to verify the correctness of the design. To run the simulation go to Assignments Menu and click Settings. In the window that pops up, under the Simulator Settings, set the Simulation Mode to Functional as shown in Figure 13. If you want to use the .do file for your simulations you can specify the file under the EDA Tool Settings->Simulation as shown in Figure 14. After these settings are done go to Tools Menu and run the EDA Simulation Tool ->EDA RTL Simulation, this will pop up the Modelsim window in which the simulation can be performed. If you are using .do file to run your simulation you need to specify the working directory where your design is compiled as shown in Figure 15.



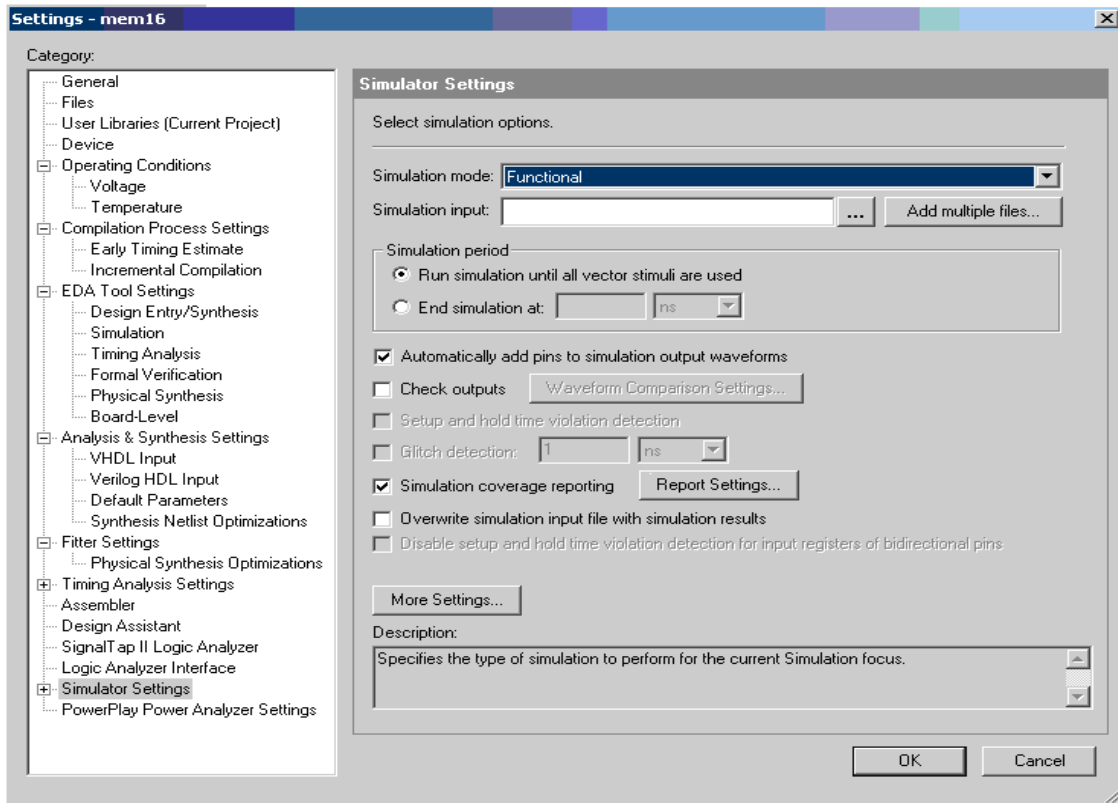


Fig. 13

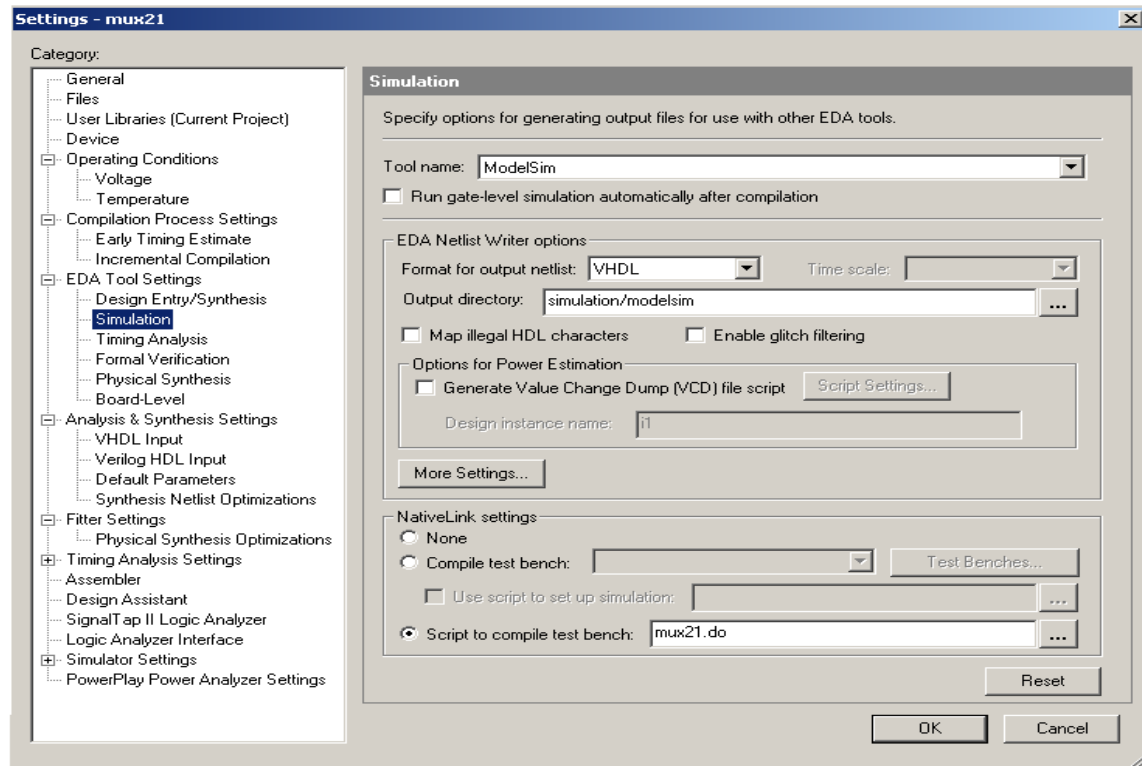
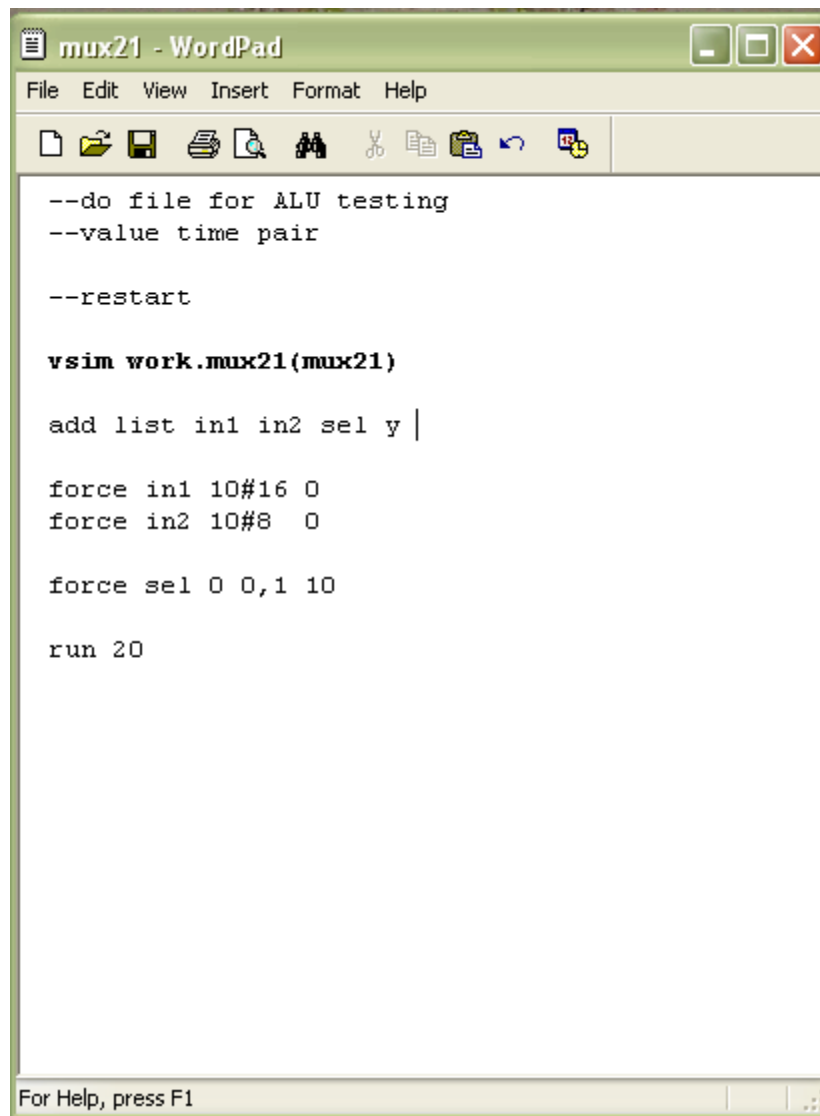


Fig. 14



```
--do file for ALU testing
--value time pair

--restart

vsim work.mux21(mux21)

add list in1 in2 sel y |

force in1 10#16 0
force in2 10#8 0

force sel 0 0,1 10

run 20
```

For Help, press F1

Fig. 15

11) During the compilation, the Quartus II Compiler was free to choose any pins on the selected FPGA to serve as inputs and outputs. However, the DE2 board has hardwired connections between the FPGA pins and the other components on the board. Pin assignments are made by using the Assignment Editor. Select Assignments > Pins to reach the window in Figure 16. Under Category select Pin to reach window in Figure 17. Double-click on the first cell which is highlighted in blue in the column labeled To. The drop-down menu in Figure 18 will appear. Choose the ports and assign the pin numbers to them from the Pin Assignment MSExcel Sheet given to you. After all the pins are assigned to save the assignments made, choose File > Save as shown in Figure 20. You can also simply close the Assignment Editor window, in which case a pop-up box will ask if you want to save the changes to assignments; click Yes. Recompile the circuit, so that it will be compiled with the correct pin assignments.

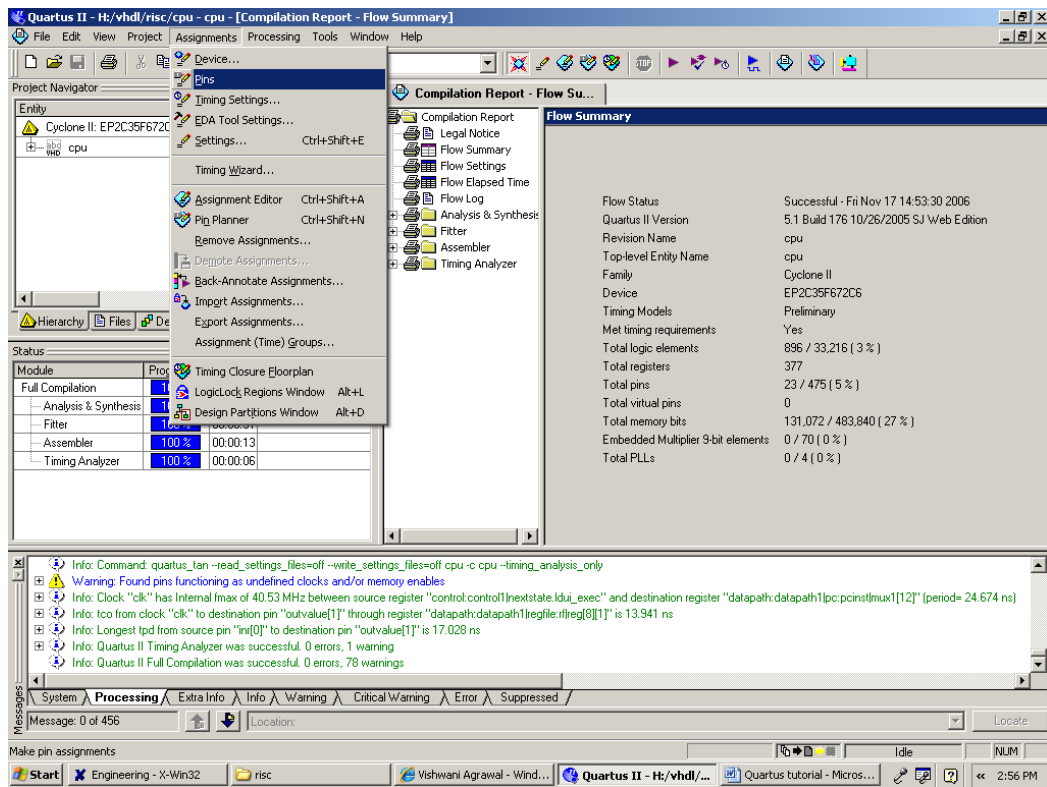


Fig. 16

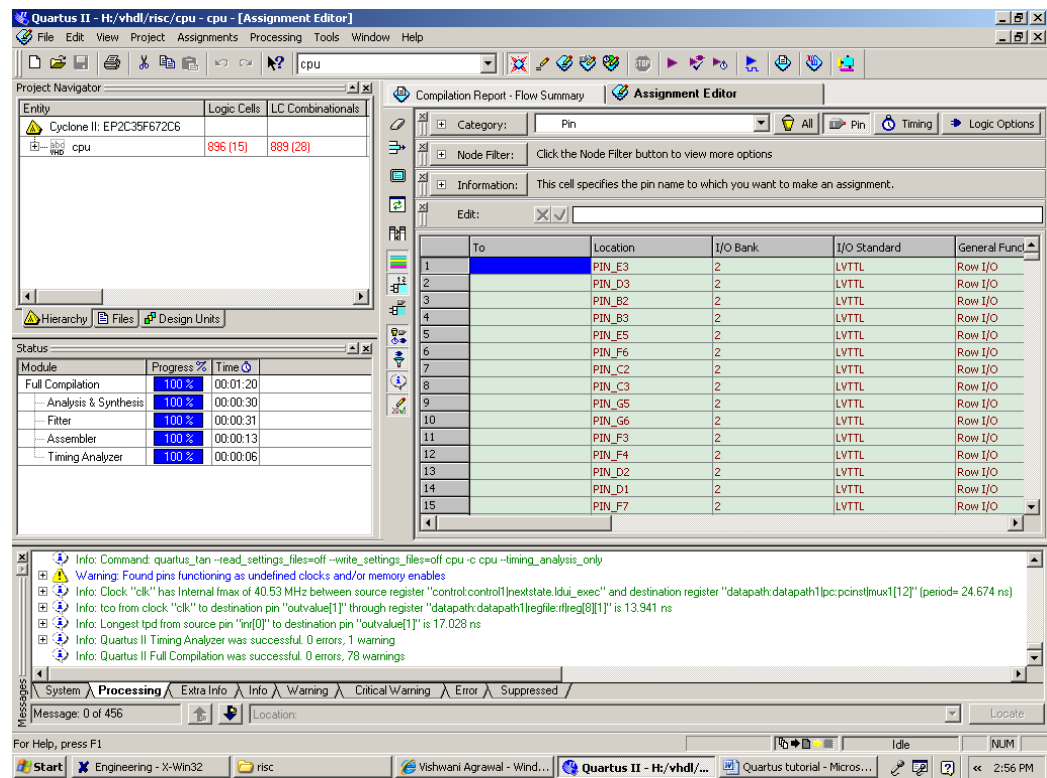


Fig. 17

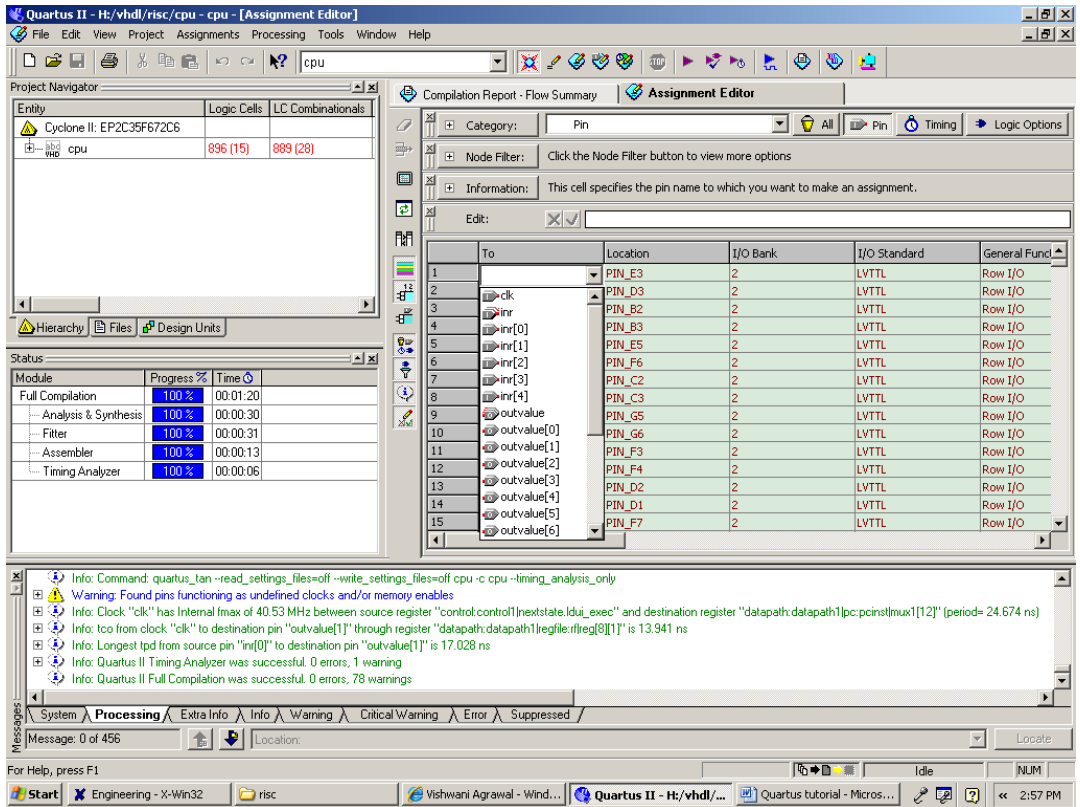


Fig. 18

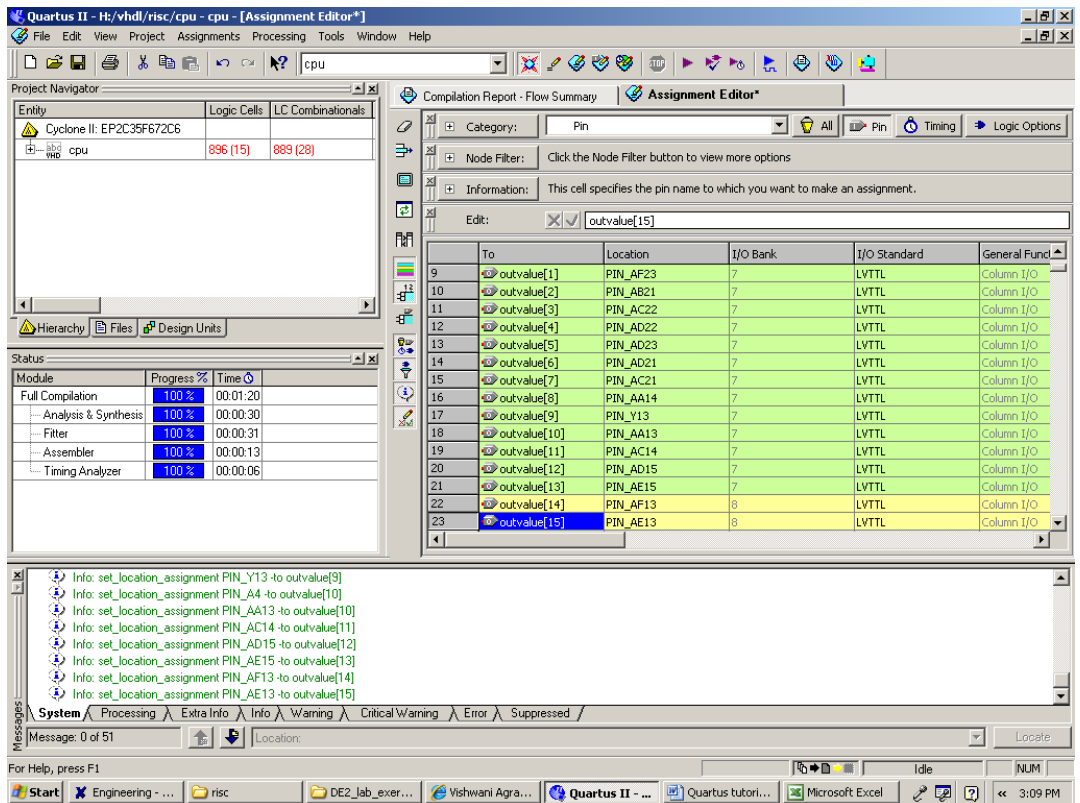


Fig. 19

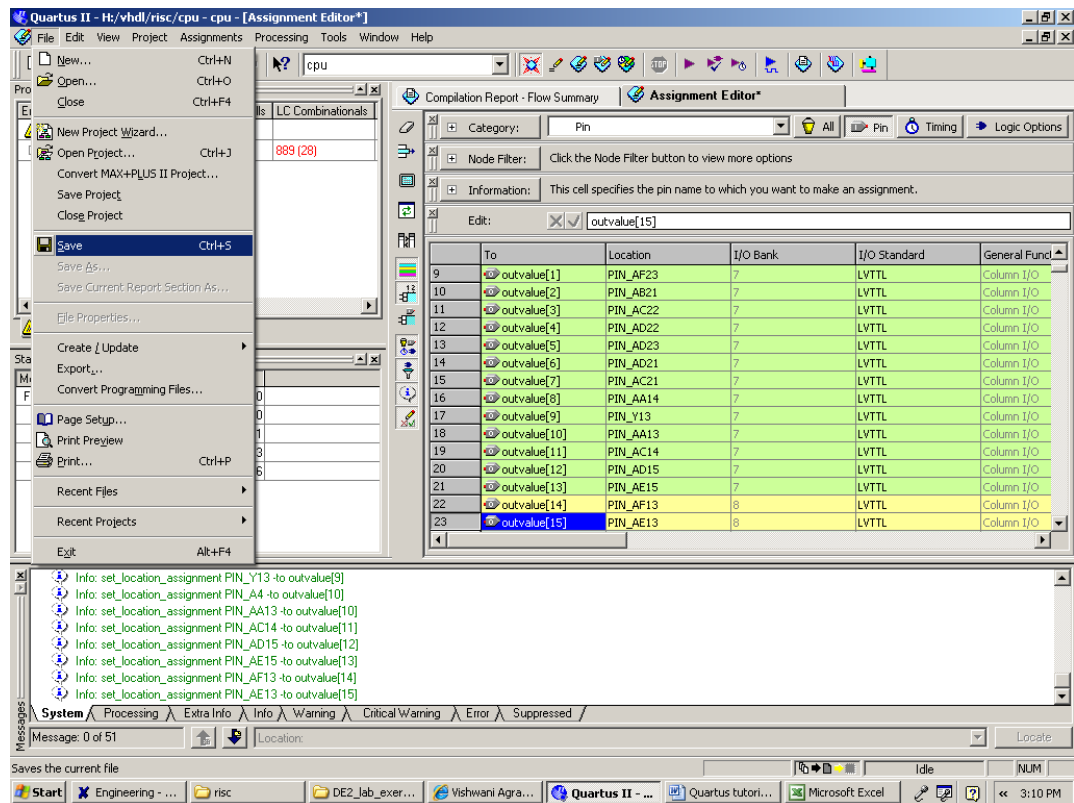


Fig. 20

12) The FPGA device must be programmed and configured to implement the designed circuit. The required configuration file is generated by the Quartus II Compiler's Assembler module. Altera's DE2 board allows the configuration to be done in two different ways, known as JTAG and AS modes. The configuration data is transferred from the host computer to the board by means of a cable that connects a USB port on the host computer to the leftmost USB connector on the board. In the JTAG mode, the configuration data is loaded directly into the FPGA device. The acronym JTAG stands for Joint Test Action Group. If the FPGA is configured in this manner, it will retain its configuration as long as the power remains turned on. The configuration information is lost when the power is turned off. The second possibility is to use the Active Serial (AS) mode. In this case, a configuration device that includes some flash memory is used to store the configuration data. Quartus II software places the configuration data into the configuration device on the DE2 board. Then, this data is loaded into the FPGA upon power-up or reconfiguration. Thus, the FPGA need not be configured by the Quartus II software if the power is turned off and on.

13) We will be using Active Serial mode of configuration. In this case, the configuration data has to be loaded into the configuration device on the DE2 board, which is identified by the name EPCS16. To specify the required configuration device select Assignments >Device, which leads to the window in Figure 21. Click on the Device & Pin Options button as shown in Fig. 22 to reach the window in Figure 23. Now, click on the Configuration tab. In the Configuration device box (which may be set to Auto) choose EPCS16 and click OK. Upon returning to the window in Figure 22, click OK. Recompile the designed circuit.

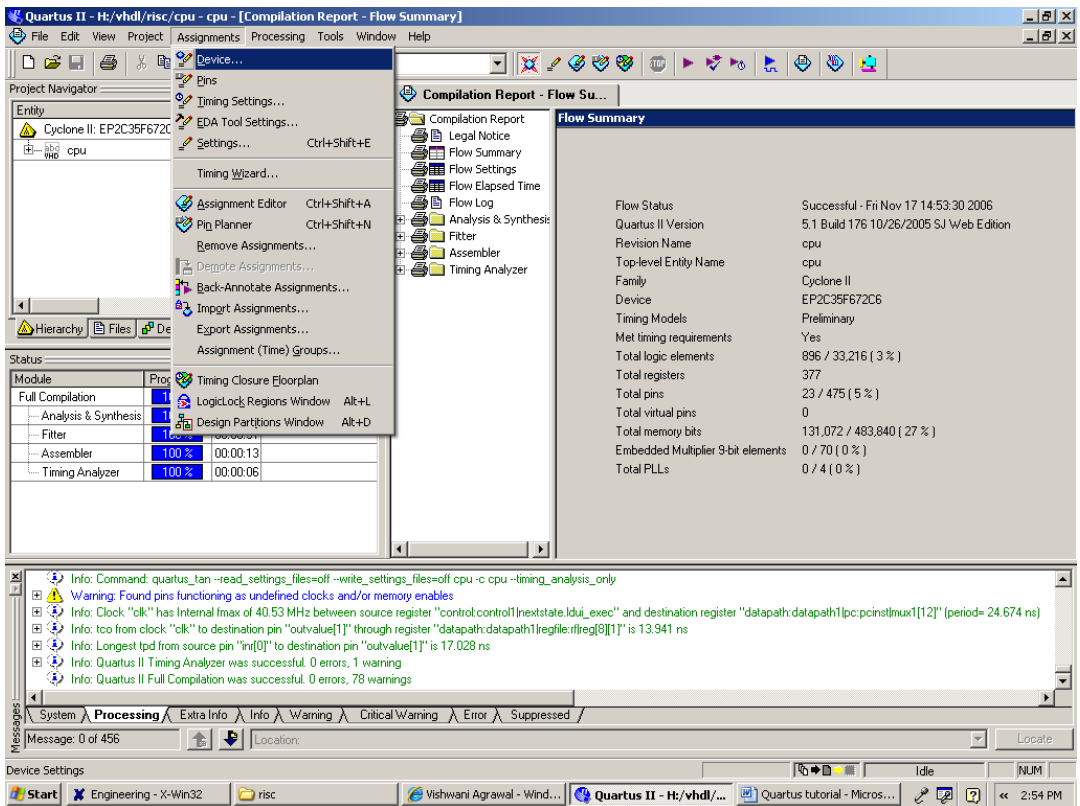


Fig. 21

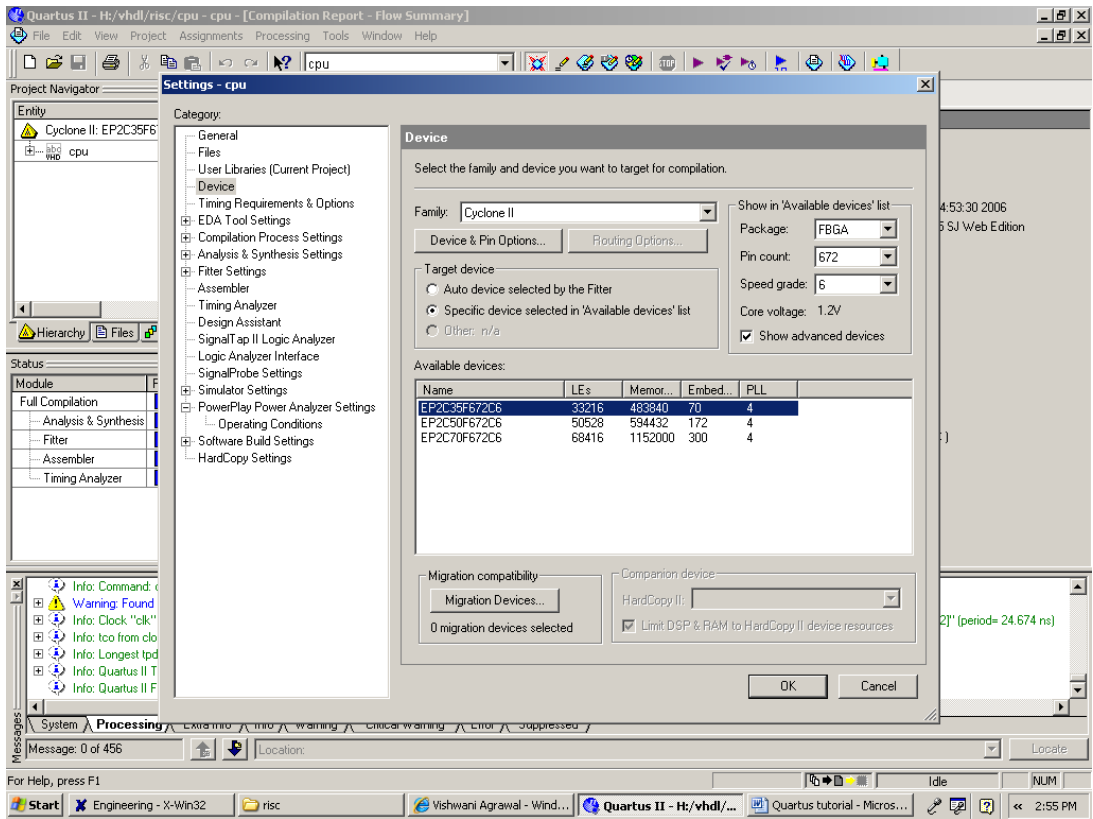


Fig. 22

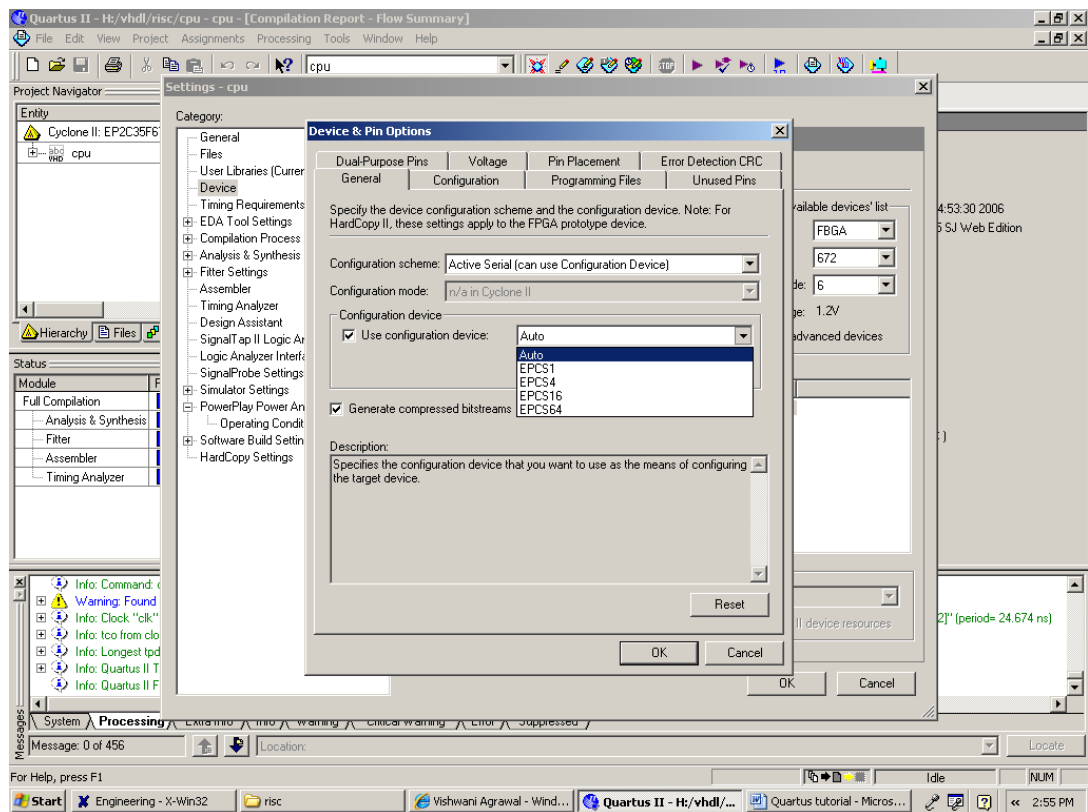


Fig. 23

14) Connect one end of the USB to the computer and second to the USB Blaster port shown in Figure 24. Also connect the Adapter to the 9V DC Power Supply Connector. Flip the RUN/PROG switch the PROG position for configuring it in AS mode. Press the Power ON/OFF switch to power up the FPGA.

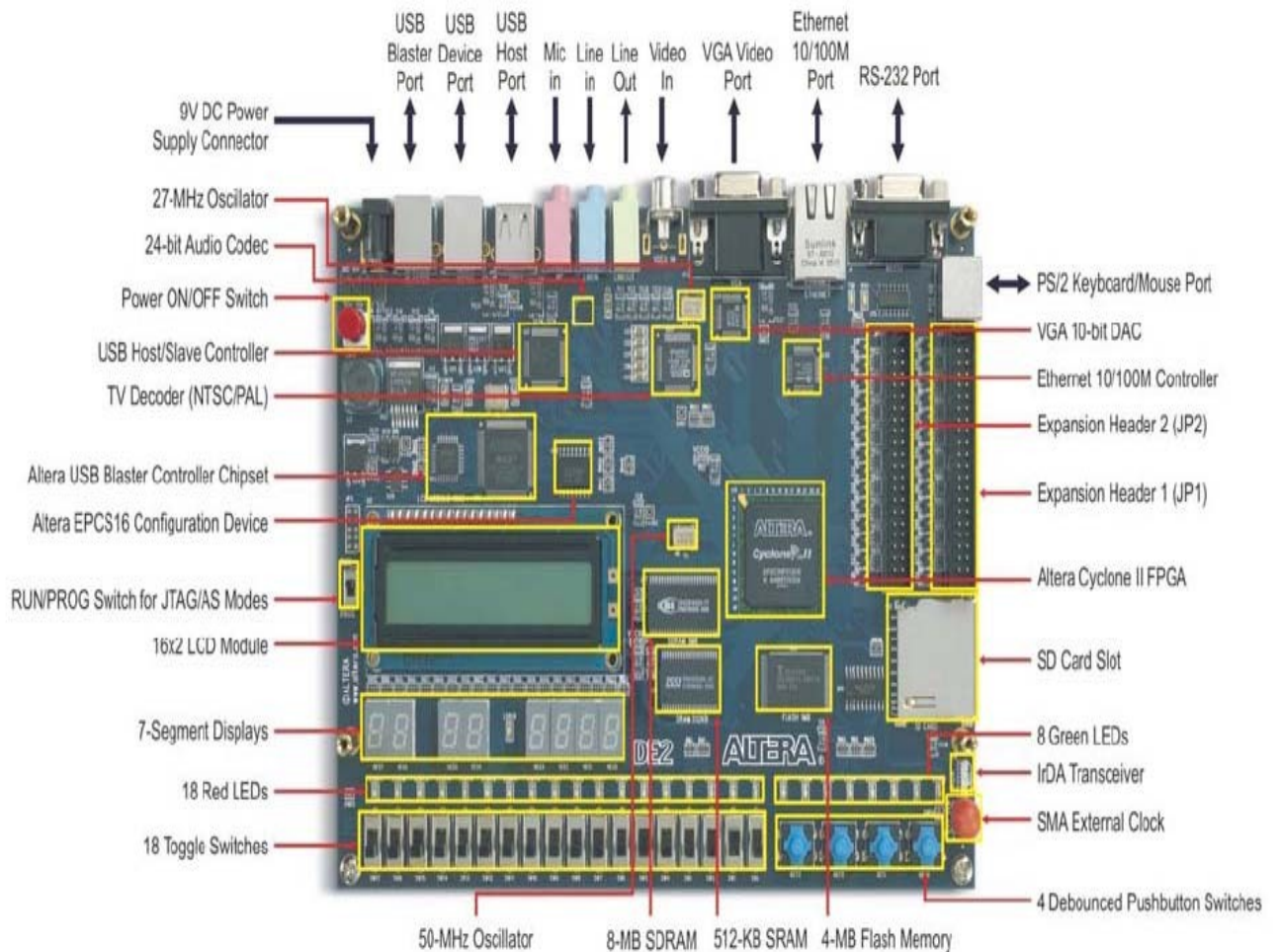


Fig. 24

15) Select Tools >Programmer to reach the window in Figure 25. In the Mode box select Active Serial Programming as shown in Fig. 26. If you are changing the mode from the previously set JTAG mode, the pop-up box will appear, asking if you want to clear all devices. Click Yes. Make sure that the Hardware Setup indicates the USB-Blaster. You can setup the Hardware as shown in Fig. 27. If the configuration file is not already listed in the window, press Add File. The pop-up box will appear. Select the file *.pof* of the project designed form your working directory and click Open. As a result, the configuration file *.pof* will be listed in the window. This is a binary file produced by the Compiler's Assembler module, which contains the data to be loaded into the EPCS16 configuration device. The extension *.pof* stands for Programmer Object File. Upon returning to the Programmer window, click on the Program/Configure check box, as shown. Press Start in the window in Figure 28. An LED on the board will light up when the configuration data has been downloaded successfully. Also, the Progress box in Figure 29 will indicate when the configuration and programming process is complete.



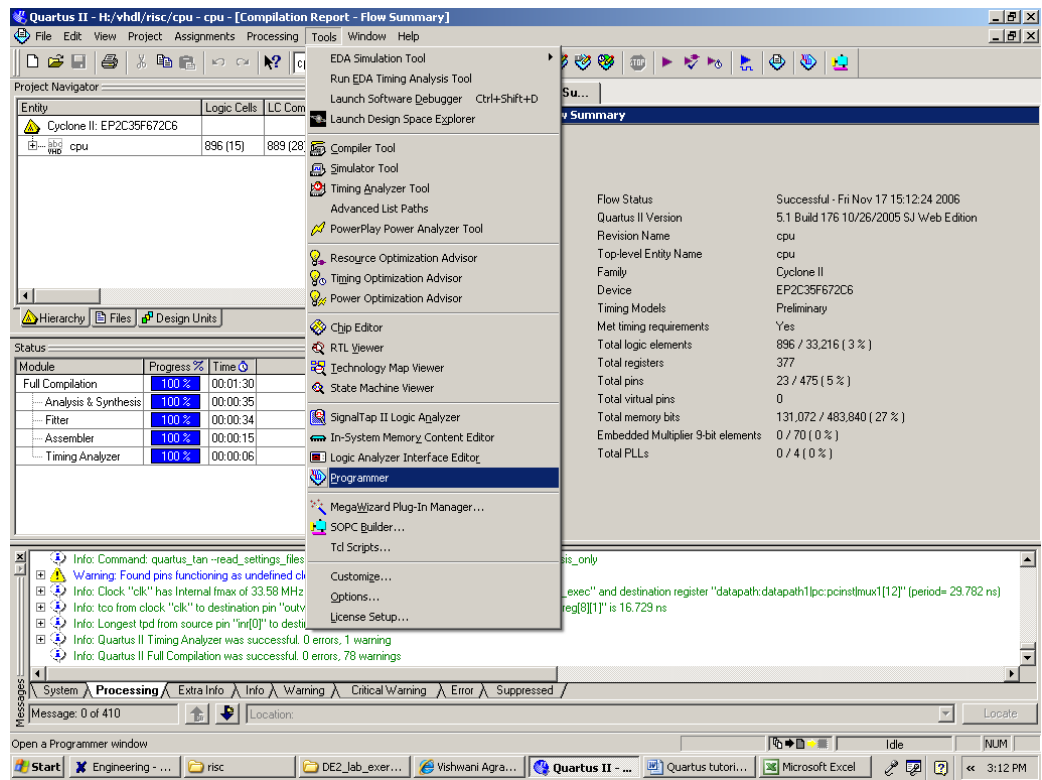


Fig. 25

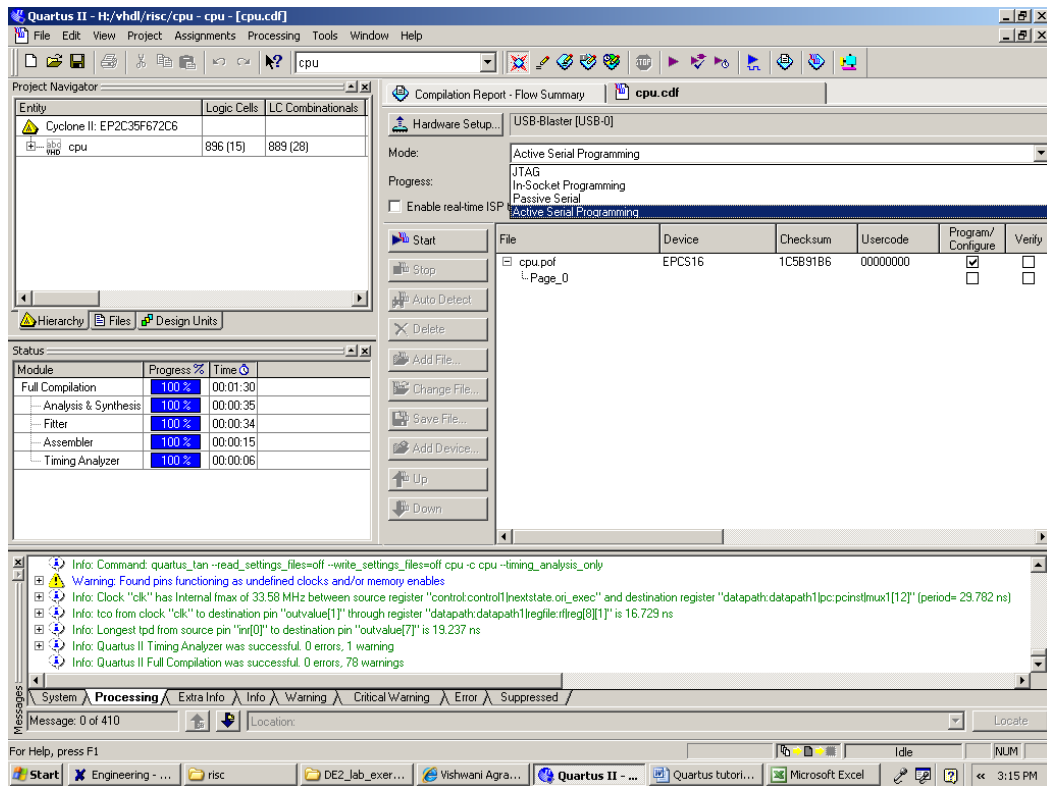


Fig. 26

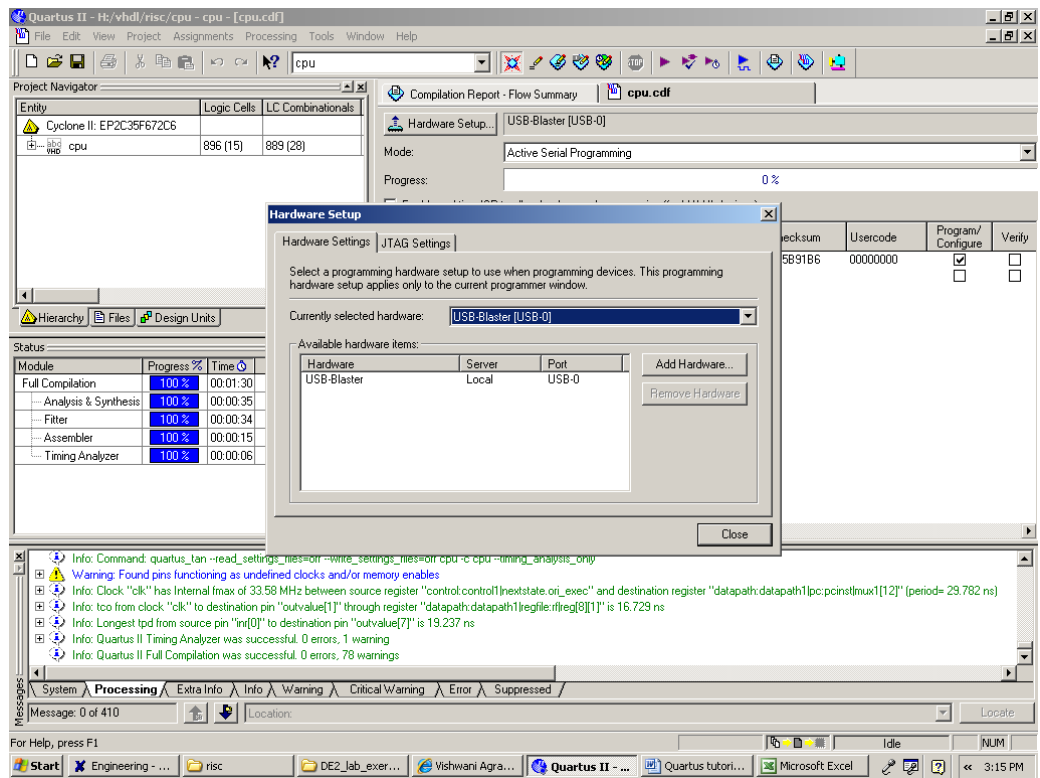


Fig. 27

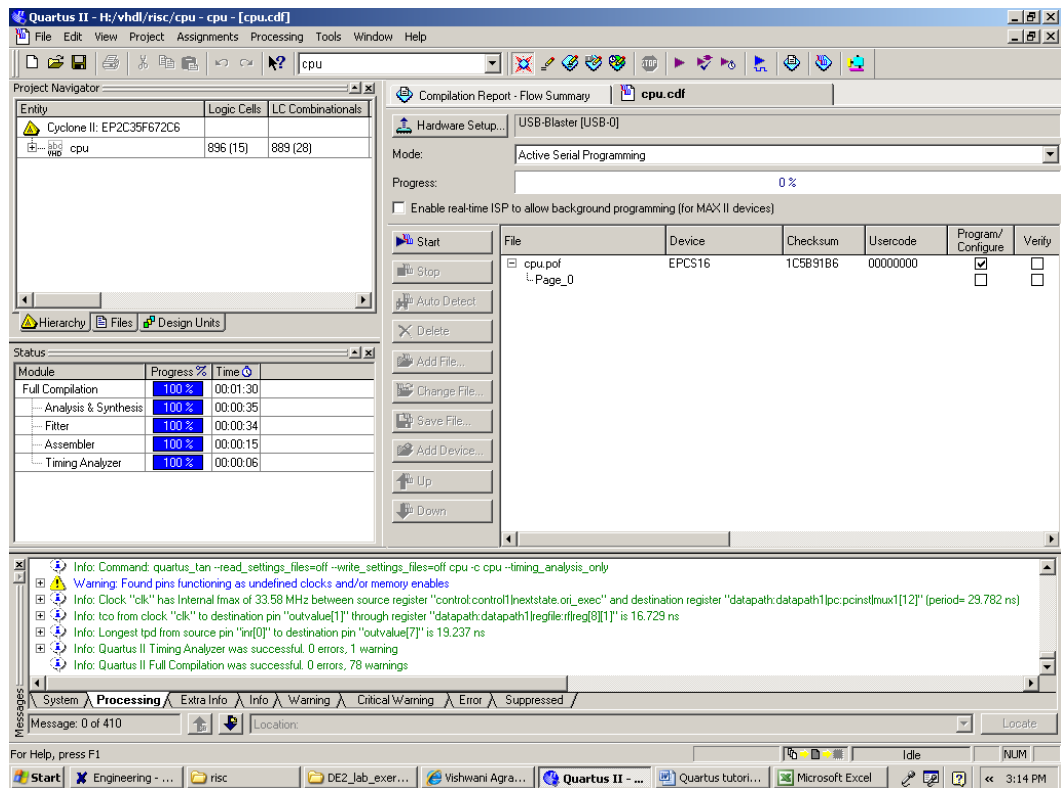


Fig. 28

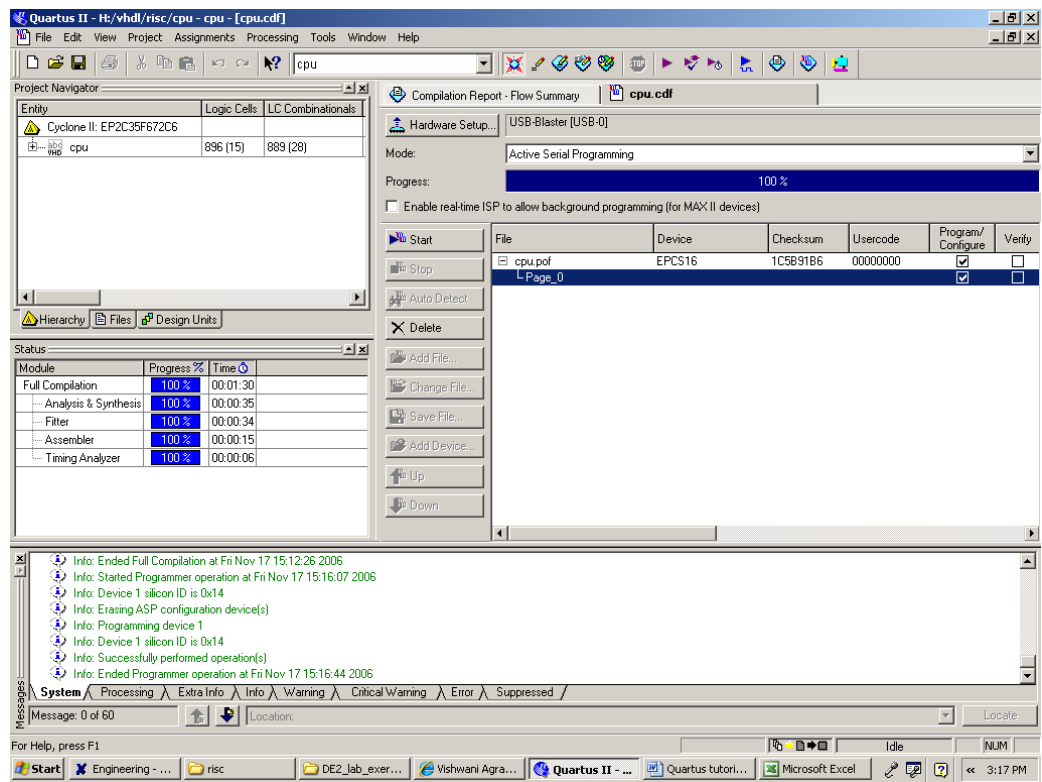


Fig. 29

16) Having downloaded the configuration data into the FPGA device, you can now test the implemented circuit. Flip the RUN/PROG switch to RUN position and Power Off the Board once and then Power up again to test it. If you want to make changes in the designed circuit, first close the Programmer window. Then make the desired changes in the VHDL design file, compile the circuit, and program the board as explained above.